## US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT, EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB: USPAT; EPO; JPO; DERWENT; IBM TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB DERWENT; IBM TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB S6 or S8 or S9 or S10 or S11 or S12 or S13 or S17 or S18 or S19 or S20 or S21 or S22 or S2US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB <u>US-PGPUB; US</u>PAT; EPO; JPO; DERWENT; IBM\_TDB JS-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; US-PGPUB; USPAT; EPO; JPO; DERWENT; US-PGPUB; USPAT; EPO; JPO; DERWENT; DERWENT; JS-PGPUB; USPAT; EPO; JPO; DERWENT; US-PGPUB; USPAT; EPO; JPO; I US-PGPUB; USPAT; EPO; JPO; JS-PGPUB; USPAT; EPO; JPO; JS-PGPUB; USPAT; EPO; JPO; JS-PGPUB; USPAT; EPO; JPO; **Databases** 8/16/05 S5 and (local\$2 with (generat\$3 or produc\$3) with (vector\$1 or stimulus or stimulii)) S5 and ((generat\$3 or produc\$3) with (vector\$1 or stimulus or stimulii)) S5 and (local\$2 with (monitor\$3 or analyz\$3 or analysis or report\$3)) EAST SEARCH S5 and ((monitor\$3 or report\$3 or test\$3) with command\$1) S5 and ((monitor\$3 or report\$3 or test\$3) with request\$1) S33 and (reconfigurable with (logic or interconnect\$1)) S5 and (reconfigurable with (logic or interconnect\$1)) S5 and (test\$3 with (vector\$1 or stimulus or stimulii)) (integrated or digital) near2 circuit\$1) with emulat\$3 ((integrated or digital) near2 circuit\$1) with emulat\$3 S31 and (distributed with (emulat\$3 or processing)) S29 and (distributed with (emulat\$3 or processing)) S3 and (distributed with (emulat\$3 or processing)) S1 and (distributed with (emulat\$3 or processing)) S5 and ((emulat\$3 near2 system) with board\$1) S5 and ((detect\$3 or report\$3) with event\$1) S5 and ((analyz\$3 or analysis) with data) S5 and (on-board with processing\$1) S5 and (on-chip with processing) S5 and (element\$1 with state\$1) S7 or S14 or S15 or S16 or S23 S33 and (circuit with element\$1) S33 and (circuit with partition\$1) S5 and (circuit with element\$1) S5 and (circuit with partition\$1) S5 and (retriev\$3 with state\$1) S5 and (board with circuit\$1) S5 and (EDA with software) circuit\$1 with emulat\$3 circuit\$1 with emulat\$3 S5 and (workstation) Search String S25 and S26 S30 or S32 S25 or S27 S2 or S4 6387 1254 59 3387 304 304 S10 \$12 \$13 \$14 \$15 \$16 \$17 **S18 S11** S2 S3 S4 S5 S6 S7 S8 S8 S8 S8

	S33 and (on-board with processing\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38 38	S33 and (element\$1 with state\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM TDB
	S33 and ((monitor\$3 or report\$3 or test\$3) with request\$1)	JPO; DERWENT;
	S33 and ((monitor\$3 or report\$3 or test\$3) with command\$1)	EPO; JPO; DERWENT; IBM
	S33 and (retriev\$3 with state\$1)	EPO.
	S33 and ((analyz\$3 or analysis) with data)	USPAT: EPO: JPO: DERWENT: IBM
	S33 and ((detect\$3 or report\$3) with event\$1)	USPAT: EPO: JPO: DERWENT: IBM
	S33 and (board with circuit\$1)	USPAT: EPO: JPO: DERWENT:
	S33 and (on-chip with processing)	USPAT: EPO: JPO: DERWENT:
	S33 and (local\$2 with (monitor\$3 or analyz\$3 or analysis or report\$3))	USPAT: EPO: JPO: DERWENT:
	S33 and (test\$3 with (vector\$1 or stimulus or stimulii))	USPAT: EPO: JPO: DERWENT: I
S51 38	S33 and ((generat\$3 or produc\$3) with (vector\$1 or stimulus or stimulii))	USPAT; EPO; JPO; DERWENT; I
	S33 and (local\$2 with (generat\$3 or produc\$3) with (vector\$1 or stimulus or stimulii))	EPO; JPO; DERWENT;
	S33 and ((emulat\$3 near2 system) with board\$1)	EPO; JPO; DERWENT;
		EPO; JPO;
	S33 and (EDA with software)	EPO: JPO: DERWENT:
	S34 or S36 or S37 or S38 or S39 or S40 or S41 or S45 or S46 or S47 or S48 or S49 or S50	EPO: JPO: DERWENT:
S57 210	S35 or S42 or S43 or S44 or S51	EPO: JPO: DERWENT:
	. S53 and S54	EPO: JPO: DERWENT: IBM
	S53 or S55	EPO; JPO; DERWENT; IBM
	6,265,894.pn. or "5,777,489".pn.	USPAT, EPO; JPO; DERWENT; IBM
	((integrated or digital) near2 circuit\$1) with emulat\$3	EPO, JPO, DERWENT, IBM
	S58 and (distributed with (emulat\$3 or processing))	USPAT: EPO, JPO: DERWENT: IBM
	S58 and (distributed with (emulat\$3 or processing))	USPAT; EPO; JPO; DERWENT; IBM
•	circuit\$1 with emulat\$3	EPO: JPO:
	S61 and (distributed with (emulat\$3 or processing))	EPO; JPO, DERWENT; IBM
•	S60 or S62	EPO; JPO;
	S63 and (reconfigurable with (logic or interconnect\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71 10	S63 and (on-chip with processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
· S72 32	S63 and (test\$3 with (vector\$1 or stimulus or stimulii))	EPO; JPO; DERWENT:
•	S63 and ((generat\$3 or produc\$3) with (vector\$1 or stimulus or stimulii))	EPO, JPO, DERWENT
S74 3	S63 and ((local\$2 or on-chip) with (generat\$3 or produc\$3) with (vector\$1 or stimulus or stimuli US-PGPUB;	USPAT; EPO; JPO; DERWENT; I
S75 53	S65 or S66 or S67 or S68	USPAT; EPO; JPO;
10/003184	Frederic Reblewski	

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**EAST SEARCH** 

Results of search set S115

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US 20050071716 A1 Testing of reconfigurable logic and interconnect sources

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Abstract

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Distributed configuration of integrated circuits in an emulation system  Neural networks decoder  Neural networks decoder  Neural networks  Emulation components and system including distributed routing and configuration of emulation teal time emulation of coherence directories using global sparse directories  Real time emulation of coherence directories using global sparse directories  Polymorphic components and system including distributed event monitoring, and testing of an IC method for detecting bus contention from RTL description  Processing device with intuitive learning capability  Hardware acceleration system for logic simulation  Processing device with intuitive learning capability  Hardware acceleration system for logic simulation  Memory circuit for use in hardware emulation system  Method analyzer for use in a hardware logic emulation system  Method and apparatus for multi-sensor processing  Method and apparatus for multi-sensor processing  Method and apparatus for multi-sensor processing  Method and apparatus for dynamically testing electrical interconnect  Intermediate-grain reconfigurable processing device  Method and system for design verification of electronic circuits  Method, apparatus, and program for multiple clock domain partitioning through retiming  Method and system for design verification of electronic circuits	Intermediate-grain reconfigurable processing device Method and apparatus for multi-sensor processing Emulation system with time-multiplexed interconnect Heuristic processor Intermediate-grain reconfigurable processing device System and method for simulation of integrated hardware and software components Emulation system with time-multiplexed interconnect Intermediate-grain reconfigurable processing device System and method for simulation of integrated hardware and software components Emulation system with time-multiplexed interconnect Intermediate-grain reconfigurable processing device Distributed logic analyzer for use in a hardware logic emulation system Method and apparatus for emulating multi-ported memory circuits Manufacturing functional testing of computing devices using microprogram based functional tes Emulation devices, systems and methods with distributed control of clock domains System and method for simulation of computer systems combining hardware and software inte Graph partitioning engine based on programmable gate arrays Electronic systems and emulation system Emulation devices, systems and methods with distributed control of test interfaces in clock don Convolutional expert neural system (ConExNS) Heuristic digital processor using non-linear transformation Method of removing gated clocks from the clock nets of a nettiist for timing sensitive implement
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bus contention from RTL description	20031218 710/107
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Heuristic processor  Convolutional expert neural system (ConExNS)  Training system for neural networks and the like  Multiple cooperating and concurrently operating processors using individually dedicated memor  Multi-layer neural network employing multiplexed output neurons  Synapse cell employing dual gate transistor structure  Solitary wave circuit for neural network emulation  Brain learning and recognition emulation circuitry and method of recognizing events  Brain emulation circuit with reduced confusion	
US 5377306 A US 5357597 A US 5222193 A US 5113500 A US 5087826 A US 4961002 A US 4896053 A US 4802103 A	